In the Specification

Amend the specification as follows:

Amend the paragraph [0025] as follows:

[0025] Above each capacitor 24, a vertical transistor is formed within the vertical trench. This is accomplished by first depositing channels 34 along the sidewalls of the trenches, which are typically doped with boron, and then growing gate oxide layers 32 thereover by thermal processing. Subsequently, there is deposited polysilicon within the remaining upper portion of each trench to form vertical gate conductors ~~34~~ 30 above the trench top oxide layer 26. The trench top oxide layer 26 insulates the gate conductor ~~34~~ 30 in the upper portion of the trenches from the storage node in the lower portion of the trenches in the DRAM arrays 10.